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Abstract
Recently, many advanced wireless communication technologies have been developed and become practical. Especially, the Orthogonal Frequency Division Multiplexing (OFDM) technique has attracted a lot of attention. Also, the OFDM technique has been applied to a number of wireless communication systems, such as Digital Audio Broadcasting (DAB), Wireless LAN IEEE 802.11 a/g, … etc. This is due to the feasibility of using the existing IFFT/FFT processors (algorithms) to carry out the OFDM coding process in the baseband processor of these communication systems. In this thesis, we use various FFT algorithms, namely, the Radix-4, Radix-4/2 and Radix-2/4/8 to implement an IFFT/FFT processor. A large number of memory components and multipliers are needed in the IFFT/FFT hardware implementation. In order to reduce the OFDM hardware implementation area and to improve its processing speed, some multiplier hardware implementation area reduction techniques are investigated. By examining the mathematical computations of IDFT(Inverse discrete Fourier Transform) and DFT(Discrete Fourier Transform), we propose a novel IFFT/FFT hardware implementation structure with less complexity for OFDM applications. In the thesis, we employ the investigated hardware implementation area reduction techniques and the proposed IFFT/FFT hardware implementation structure to implement area efficiency OFDM processors. In the implementation procedures, MATLAB is first used to verify the OFDM function. The hardware design and simulation are then carried out by Verilog HDL coding. Finally, the OFDM chip is implemented by a digital IC design flow (Cell base Flow). The hardware area of the implemented OFDM chip is reduced substantially and its processing speed is also improved. Based on the proposed IFFT/FFT hardware structure and area reduction techniques, a configurable number of subcarrier (64 to 8192) of OFDM chip is designed by employing a combination structure of the radix-4 and radix-2 FFT algorithms.
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